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June 8, 2000

Attorney Docket No.: 08305/081001/98-29

**Box Patent Application**  
Commissioner for Patents  
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: ALEXANDER I. KRYMSKI

Title: A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	14
Claims	6
Abstract	1
Declaration	2
Drawing(s)	7

Enclosures:

- Assignment cover sheet and an assignment, 2 pages, and a separate \$40 fee.
- Small entity statement. This application is entitled to small entity status.
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Page 2

There are 21 total claims, 3 independent.

Basic filing fee	\$345
Total claims in excess of 20 times \$9	\$9
Independent claims in excess of 3 times \$39	\$0
Fee for multiple dependent claims	\$0
Total filing fee:	\$354

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

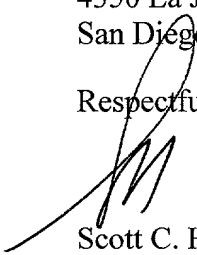
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Respectfully submitted,

  
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ATTORNEY DOCKET NO. 08305/081001

Applicant or Patentee: Alexander Krymski

Serial or Patent No.: \_\_\_\_\_

Filed or Issued: \_\_\_\_\_

For: A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS  
(37 CFR 1.9(f) and 1.27(e)) — SMALL BUSINESS CONCERN**

I hereby declare that I am

- ☐ the owner of the small business concern identified below:  
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: PHOTOBIT CORPORATIONAddress of Small Business Concern: 135 North Los Robles Avenue, 7th Floor  
Pasadena, California 91101

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS by inventor(s) ALEXANDER I. KRYMSKI described in:

- ☒ the specification filed herewith.  
☐ application serial no. \_\_, filed \_\_.  
☐ patent no. \_\_, issued \_\_.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below\* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e). \*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

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I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

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Name:	<u>Angela L. McNamee</u>
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APPLICATION  
FOR  
UNITED STATES LETTERS PATENT

TITLE: A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS  
APPLICANT: ALEXANDER I. KRYMSKI

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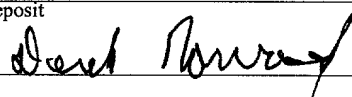
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June 8, 2000

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Derek Norwood

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A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS

**BACKGROUND**

The present disclosure generally relates to image  
5 sensors, and specifically to a low-power signal chain in  
such sensors.

Image sensors can be applied in a variety of fields,  
including machine vision, robotics, guidance and  
navigation, automotive applications, and consumer products.  
10 In "smart" image sensors, it is often desirable to  
integrate on-chip circuitry to control the image sensor and  
to perform signal and image processing on the output image.

Active pixel sensors (APS), which have one or more  
active transistors within the pixel unit cell, can be made  
15 compatible with CMOS technologies. An active pixel sensor  
is often arranged as an array of elements referred to as a  
pixel array. Each column of the array can be read out at  
one time, driven and buffered for sensing by a signal chain  
including a readout circuit, an output stage, and an A-to-D  
20 converter.

**SUMMARY**

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The present disclosure defines a signal chain for an image sensor. The signal chain includes photo sensing elements, pixel readout circuits, and an amplifier. Each pixel readout circuit receives a charge-induced signal and a reset signal from a photo-sensing element. The readout circuit computes a difference signal between the charge-induced signal and the reset signal. The difference signal is measured with respect to a reference. The amplifier is coupled to the pixel readout circuits, and configured to supply the reference during computation of the difference signal. Further, the amplifier amplifies the difference signal when the computation is completed.

The present disclosure further includes a method for pixel readout. The method includes reading a charge-induced signal and a reset signal from a first series of pixels. The method also includes computing a first difference signal between the charge-induced signal and the reset signal, and enabling a first A-to-D converter to convert the first difference signal to a first digital value. The method further reads another charge-induced signal and another reset signal from a second series of pixels while the first A-to-D converter is performing conversion. A second difference signal between another charge-induced signal and another reset signal is then computed. Finally, a second A-

to-D converter converts the second difference signal to a second digital value.

An image sensor circuit further includes a pixel array addressing circuit and a controller.

5

#### BRIEF DESCRIPTION OF THE DRAWINGS

Different aspects of the disclosure will be described in reference to the accompanying drawings wherein:

FIG. 1 is an exemplary conventional signal chain;

10      FIG. 2A shows a low-power signal chain in accordance with an embodiment of the present system;

FIG. 2B shows a sample-and-hold circuit for the reference voltage generator in accordance with an embodiment of the present invention;

15      FIG. 2C is a schematic diagram of the sample-and-hold circuit shown in FIG. 2B;

FIGS. 2D and 2E show output plots of an amplifier without and with the sample-and-hold circuit inserted into the voltage reference generator, respectively;

20      FIG. 3 is a block diagram of a multiplexer connected to two A-to-D converter according an embodiment of the present system;

FIG. 4 shows an example of a CMOS image sensor integrated circuit chip; and

FIG. 5 shows an example of an image sensor pixel array with output stage.

#### DETAILED DESCRIPTION

5       The operation of an exemplary signal chain 100 of FIG. 1 is explained below. In general, the signal chain operates in a double sampling differential mode.

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10       The signal value on a photosensitive pixel element 104 is switched through the source-follower transistor 106 and the transistor 110 to the capacitor  $C_1$ . After the capacitor  $C_1$  is charged to the proper voltage, the photosensitive element 104 is reset using the reset switch 108. The reset level of the pixel 101 is sampled by the transistor 112, and stored on the capacitor  $C_2$ . The negative plates of the  
15       capacitors  $C_1$ ,  $C_2$  can be clamped during appropriate times. The capacitors are clamped at a reference voltage ( $V_{REF}$ ) by closing associated switches 122, 124, respectively.

20       After the initial sampling steps, the capacitors  $C_1$  and  $C_2$ , respectively, hold signal and reset values. The signal and reset values are sent from the respective column readout circuits 120 to the output stage 130 through a pair



of column select switches 114, 116. The column readout circuits 120 are read sequentially, e.g. one at a time.

When the switches 114, 116 are first turned on, the integrators 132, 134 are held in reset by the switches 136, 138. Resetting the switched integrators 132, 134 erases any previously-stored signals. The reset action also restores the reference voltage ( $V_{REF}$ ) to the inverting inputs of the integrators 132, 134. Substantially simultaneously, the crowbar transistor 118 is turned on to short together the common sides of capacitors  $C_1$ ,  $C_2$ . This provides charge from capacitors  $C_1$ ,  $C_2$  through the respective switches 114, 116 and to the integrators 132, 134. The charge from the capacitors  $C_1$ ,  $C_2$  is coupled onto the integrators' capacitors  $C_3$ ,  $C_4$ . The effect is that the charge is driven through the circuit of the system and offsets are reduced.

Once the signal and reset values stored in one of the column readout circuits 120 has been read by the output stage 130, the values are converted to a digital signal by an A-to-D converter 140. The signal and reset values stored in other column readout circuits can be read sequentially by the output stage. When all the pixels from the selected row have been read by the output stage 130,

the process can be repeated for a new row of pixels in the pixel array.

The present system defines a low-power signal chain for a CMOS image sensor. One embodiment of the low-power signal chain 200 in accordance with the present system is shown in FIG. 2A. The signal chain 200 includes a column readout circuit 210, an output charge detection amplifier 220, and a capacitive successive approximation A-to-D converter system 230.

All pixels in a column are connected in parallel with switching circuits that control which of the pixels of the column is output at any one time. The signal from each selected pixel circuit 201 arrives at the column input 204. The signal is typically a negative charge amount that subtracts from the high level reset.

The active pixel sensor pixel circuit 201 includes a photosensor 203, and an in-pixel follower amplifier 205. Photosensor 203 can include, for example, a photodiode, a photogate or a charge injection device. The output signal 202 is a sequence of low (signal) and high (reset) voltages. The output is connected to capacitors  $C_1$ ,  $C_2$  that carry out a sampling operation between the output voltages that are output at different times.

A typical double sampling operation first samples the output voltage. That voltage is the level of the reset.

Next output voltage is the level of the photo-charge-induced signal, added to the supply voltage, here  $V_{DD}$ .

During the time that the pixel signal 202 is "active", metal oxide semiconductor field-effect transistors (MOSFET) 212, 214 and a switch 222 are all turned on (closed). This applies the signal to the stages 210 and 220. The sample and hold (S/H) transistor 212 is maintained on during that time by the S/H voltage that drives the gate of the transistor 212. While the S/H voltage is high, the charge-induced voltage passes through the sample and hold transistor 212, and is accumulated by the capacitors  $C_1$ ,  $C_2$ . The capacitor  $C_1$  is connected from S/H node 216 to the ground and the second capacitor  $C_2$  is connected in series with S/H transistor 212.

When the column selection transistor 214 is on, the negative plate of  $C_2$  is charged to the voltage at the negative input node 224 of the amplifier 228. With the feedback switch 222 closed, the negative input node 224 of the amplifier 228 settles to about the same level as the reference voltage ( $V_{REF}$ ) at the positive input node 226. The negative plate of the pass-through capacitor  $C_2$  may otherwise need clamping to a reference voltage. Other advantages include substantial reduction in switch feed-through error caused by sample and hold transistor 212 and offset errors caused by a reference voltage.

Once the pixel signal 202 is sampled, the column selection switch 214 is turned off. The reset voltage may be sampled onto the capacitor  $C_1$ . The capacitor  $C_2$  then settles to a charge related to a signal level minus a reset level. When the column selection switch 214 is turned on again, the difference signal of the result (signal minus reset plus reference) is applied to the inverting amplifier stage 220 that includes feedback capacitor  $C_3$ .

For low voltage operation, the transistor switch 212 operates with signal close to the ground, while the transistor switch 214 passes a reference voltage from amplifier close to the supply voltage. Therefore, it is preferred that transistor switches 212 and 214 be n-channel MOSFET (NMOS) transistor and p-channel MOSFET (PMOS) transistor, respectively.

The amplifier circuit 220 includes an op-amp 228, which uses a voltage reference ( $V_{REF}$ ) that biases the op-amp 228 to a desired operating point. The op-amp 228 is preferably a trans-impedance op-amp that extends the dynamic range of the signals. The value of the reference voltage is selected to be about 0.5 volts below the supply voltage ( $V_{DD}$ ).

The amplifier circuit 220 further includes a feedback switch 222 and a feedback capacitor  $C_3$ . The gain ( $G$ ) of the charge sensing amplifier circuit 220 is determined by the capacitance that is selectively coupled to an inverting input 224 of the op-amp 228 through the column selection

transistor 214. Therefore, the gain of the amplifier circuit is approximately equal to the ratio of the effective capacitance seen by the inverting terminal 224 of the op-amp 228 and the value of the feedback capacitor  $C_3$ .

5 To achieve low-noise operation in the column readout circuit 210 and the amplifier circuit 220, the voltage reference ( $V_{REF}$ ) needs to be substantially stable. In particular, the signal ripple during critical operational periods should be substantially less than the fundamental  
10 noise, such as shot noise or dark signal noise, in the sensor. The critical periods include pixel signal sampling, amplifier reset, and column charge readout. Thus, given the desired stability for the reference voltage during one row time, a sample-and-hold circuit shown in FIG. 2B is provided  
15 for the reference voltage.

The sample-and-hold circuit includes a voltage reference generator 280, a plurality of switches 282, 284, and a charge capacitor  $C_4$ . The voltage reference generator 280 generates a reference voltage, which may be noisy. The  
20 switches 282, 284 operate to sample the generated reference voltage onto the charge capacitor  $C_4$ . The reference voltage is sampled onto the charge capacitor  $C_4$  at the beginning of each row sample time. The sampling switch 282 is then opened while the sampled voltage is held constant by the  
25 charge capacitor  $C_4$  until the next row sample time. Since the sampling period is short compared to the entire row

select period, the sample-and-hold circuit also saves power for the amplifier circuit 220. The output of the sample-and-hold circuit 226 is connected to the positive input of the amplifier 228 in the amplifier circuit 220.

5 In one implementation of the sample-and-hold circuit, shown in FIG. 2C, the voltage reference generator 280 is implemented with two resistors  $R_1$ ,  $R_2$  configured as a voltage divider. Since the values of  $R_1$  and  $R_2$  are  $10K\Omega$  and  $20 K\Omega$  respectively, the generated reference voltage is  
10 about 67% of the supply voltage,  $V_{DD}$ . The switches may be implemented with p-channel 290 and n-channel MOSFET transistors 292. The capacitor  $C_s$  may be 10 pF.

FIG. 2D is an output plot of the amplifier showing the sample and reset signals. The plot was generated without  
15 the sample-and-hold circuit. The plot shows the voltage ripple on the order of about 10 mV, which corresponds to about 5%.

FIG. 2E is an output plot of the same amplifier with the sample-and-hold circuit inserted into the voltage  
20 reference generator. The plot shows the negligible ripple on the output of the amplifier.

The amplified differential analog signal is then converted to a corresponding digital data by A-to-D converter system 230. For one embodiment, the A-to-D  
25 converter system 230 includes two comparators 232, 234 and a

binary-scaled network of capacitors 236, 238. A "strobe" signal enables the comparators 232, 234 to provide an output signal based on the signals at its positive and negative terminals. The binary-scaled capacitor network 236, 238 is used to approximate the amplified differential pixel signal using a successive approximation technique.

The result of the comparison for the binary-scaled capacitor network 230 is stored by the associated one of the latches 240, 242. The values of the digital bits corresponding to the analog differential pixel signal are stored by the respective latches 240, 242 while the amplification and conversion steps are performed for the pixel 201.

For readout, the amplifier 220 is initially preset by closing the switch 222 and sampling this reset level onto the capacitor 244 through the switch 250. A column readout circuit 210 is connected to the amplifier 220 through the column selection switch 214. The pixel signal 202 is injected onto the binary-scaled capacitor 236 when the switch 252 is closed. The first A-to-D converter 260 then enters a conversion mode in which the binary-scaled capacitor 236 is successively programmed to convert the amplified differential signal. The switches 250, 252 are turned off during this conversion mode.

Substantially simultaneously with the beginning of the conversion mode of the first A-to-D converter 260, the

amplifier 220 is again preset by closing the switch 222. This reset level is sampled onto the capacitor 246 through the switch 254. Another column readout circuit 270 is then connected to the amplifier 220 through another column selection switch. The pixel signal corresponding to this new column is injected onto the binary-scaled capacitor 238 when the switch 256 is closed. The second A-to-D converter 262 is in a sampling mode when the first A-to-D converter 260 is in a conversion mode.

FIG. 3 illustrates an advantage of the present system. A multiplexer 300 alternately outputs digital data produced by latches 240, 242 in the A-to-D converters 260, 262, respectively. The two A-to-D converters 260, 262 alternately perform sampling and conversion. Therefore, this configuration of having two A-to-D converters in a system 230 enables outputting of a continuous data stream without using extra memory.

FIG. 4 shows an example of a CMOS image sensor integrated circuit chip 400. The chip 400 includes an array of active pixel sensors 402 and a controller 404. The controller 404 provides timing and control signals to enable read out of signals stored in the pixels. For some embodiments, arrays can have dimensions of 128x128 or larger number of pixels. However, in general, the size of the array 402 will depend on the particular implementation. The image array 402 is read out a row at a time using column-



parallel readout architecture. The controller 404 selects a particular row of pixels in the array 402 by controlling the operation of vertical addressing circuit 406 and row drivers 408. Charge signals stored in the selected row of pixels are provided to a readout circuit 410. The pixels read from each of the columns can be read out sequentially using a horizontal addressing circuit 414. Differential pixel signals ( $V_{in}^+$ ,  $V_{in}^-$ ) are provided at the output of the readout circuit 410. The differential pixel signals are sent to at least two A-to-D converters 412 to be converted to digital values. The readout circuit 410 and the A-to-D converter system 412 forms a low-power signal chain that performs sample and hold operation.

As shown in FIG. 5, the array 402 includes multiple columns 500 of CMOS active pixel sensors 502. Each column includes multiple rows of sensors 502. Signals from the active pixel sensors 502 in a particular column can be read out to a readout circuit 504 associated with that column. Signals stored in the readout circuits 504 can be read to an output stage 506. This output stage 506 is common to the entire array of pixels 402. A-to-D converters 508, 510 convert analog signals to digital data. Multiplexer 512 successively strobes converted digital data into a stream of output data.

Some of the advantages of the present system are illustrated in FIG. 5 described above. The figure shows the

reference voltage 514 being supplied to the output stage 506 instead of the column readout circuits 504 for all columns in the prior art system. Further, since the reference voltage 514 is applied to a high-impedance node (see FIG.

5 2A) of the op-amp, the current consumption in the present system is significantly less than that of the prior art system. Hence, the present system provides low-power signal chain for a CMOS active pixel sensor.

Other embodiments and variations are possible. For  
10 example, in a compact chip design, the capacitors C1 and C2 can be implemented as MOSFET capacitors.

All these are intended to be encompassed by the following claims.

**What is claimed is:**

1           1.    A signal chain for an image sensor, comprising:  
2           a plurality of photo sensing elements;  
3           a plurality of pixel readout circuits, each pixel readout  
4           circuit operating to receive a charge-induced signal and a reset  
5           signal from a photo sensing element, and to compute a difference  
6           signal between said charge-induced signal and said reset signal,  
7           said difference signal being measured with respect to a reference  
8           signal; and

          an amplifier configured to receive said reference signal,  
          and to supply said reference signal to said plurality of pixel  
          readout circuits during computation of said difference signal,  
          where said amplifier amplifies said difference signal when the  
          computation is completed.

          2.    The signal chain of claim 1, further comprising:  
          a plurality of A-to-D converters operating to alternately  
          convert said amplified difference signal.

          3.    The signal chain of claim 2, wherein each of said  
          plurality of A-to-D converters includes a binary-scaled capacitor  
          network capable of sampling and converting said reference signal  
          to a digital value.

1           4.    The signal chain of claim 3, wherein said each of said  
2   plurality of A-to-D converters includes a latch to save the  
3   converted difference signal.

1           5.    The signal chain of claim 3, wherein said plurality of  
2   A-to-D converters includes:

3           a first A-to-D converter arranged into a first configuration  
4   operating to convert said amplified difference signal in a  
5   particular cycle; and

6           a second A-to-D converter arranged into a second  
configuration operating to sample a next amplified difference  
signal into said binary scaled capacitor network in said  
particular cycle,

          wherein said first and said second A-to-D converters switch  
configurations in a cycle after said particular cycle.

6           6.    The signal chain of claim 2, further comprising:  
          a multiplexer configured to sequentially output saved  
3   difference signal in said latch.

1           7.    The signal chain of claim 1, wherein said plurality of  
2   photo sensing elements is a pixel array arranged in columns of  
3   pixels.

1           8.    The signal chain of claim 1, wherein said each pixel  
2    readout circuit includes at least two capacitive elements, one to  
3    hold pixel reset value, and another to compute and store said  
4    difference signal between said charge-induced signal and said  
5    reset signal.

1           9.    The signal chain of claim 1, wherein said amplifier  
2    includes a feedback switch operating to provide said reference  
3    signal, received at a negative input to said amplifier, to said  
4    each pixel readout circuit through a feedback.

1           10.   The signal chain of claim 1, wherein said each pixel  
2    readout circuit includes a column select switch to connect  
3    selected column pixel readout to said amplifier.

1           11.   The signal chain of claim 10, wherein said column  
2    select switch is a p-channel MOSFET (PMOS) transistor.

1           12.   The signal chain of claim 1, wherein said each pixel  
2    readout circuit includes a sample and hold switch to sequentially  
3    read said charge-induced signal and said reset signal.

1           13.   The signal chain of claim 12, wherein said sample and  
2    hold switch is an n-channel MOSFET (NMOS) transistor.

1 14. The signal chain of claim 1, further comprising:  
 2 a sample and hold circuit coupled to said reference signal,  
 3 said sample and hold circuit operating to provide stable  
 4 reference signal.

1 15. The signal chain of claim 14, wherein said signal  
 2 smoothing circuit includes:

3 a reference signal generator operating to generate the  
 4 reference signal;

5 at least one switch configured to sample and hold the  
 reference signal at a certain level; and

a capacitor coupled to said at least one switch, said  
 capacitor operating to hold the sampled value at the certain  
 level.

16. The signal chain of claim 15, wherein said reference  
 signal generator includes a voltage divider resistor network.

1 17. The signal chain of claim 15, wherein said at least one  
 2 switch includes MOSFET transistors.

1 18. An image sensor output circuit, comprising:  
2 a pixel array having a series of pixels, and operating to  
3 receive optical data and convert said optical data into  
4 electrical signals;  
5 readout circuits configured to read said electrical signals  
6 from said series of pixels with respect to a reference signal;  
7 an amplifier configured to provide said reference signal  
8 while said readout circuit is reading said electrical signal, and  
9 to provide amplification of said referenced electrical signals  
10 when the reading is done; and  
11 at least one A-to-D converter operating to provide  
12 conversion of said amplified electrical signal.

13 19. The circuit of claim 18, wherein said at least one A-  
14 to-D converter includes first and second A-to-D converters, said  
15 first A-to-D converter converting said reference electrical  
16 signal while said second A-to-D converter is sampling a next  
17 reference electrical signal.

18 20. The circuit of claim 18, further comprising:  
19 a multiplexer configured to sequentially output converted  
20 signals.

21. An image sensor comprising:

a pixel array having a plurality of pixels;

a plurality of pixel readout circuits, each pixel  
readout circuit operating to receive a charge-induced signal  
and a reset signal from a pixel of said pixel array, and to  
compute a difference signal between said charge-induced  
signal and said reset signal, said difference signal being  
measured with respect to a reference signal;

an amplifier coupled to said each pixel readout  
circuit, said amplifier configured to supply said reference  
signal during computation of said difference signal, and to  
amplify said difference signal when the computation is done;

a pixel array addressing circuit configured to select a  
group of pixels in said pixel array to readout; and

a controller coupled to said pixel array addressing  
circuit, and operating to provide selection control to said  
pixel array addressing circuit.

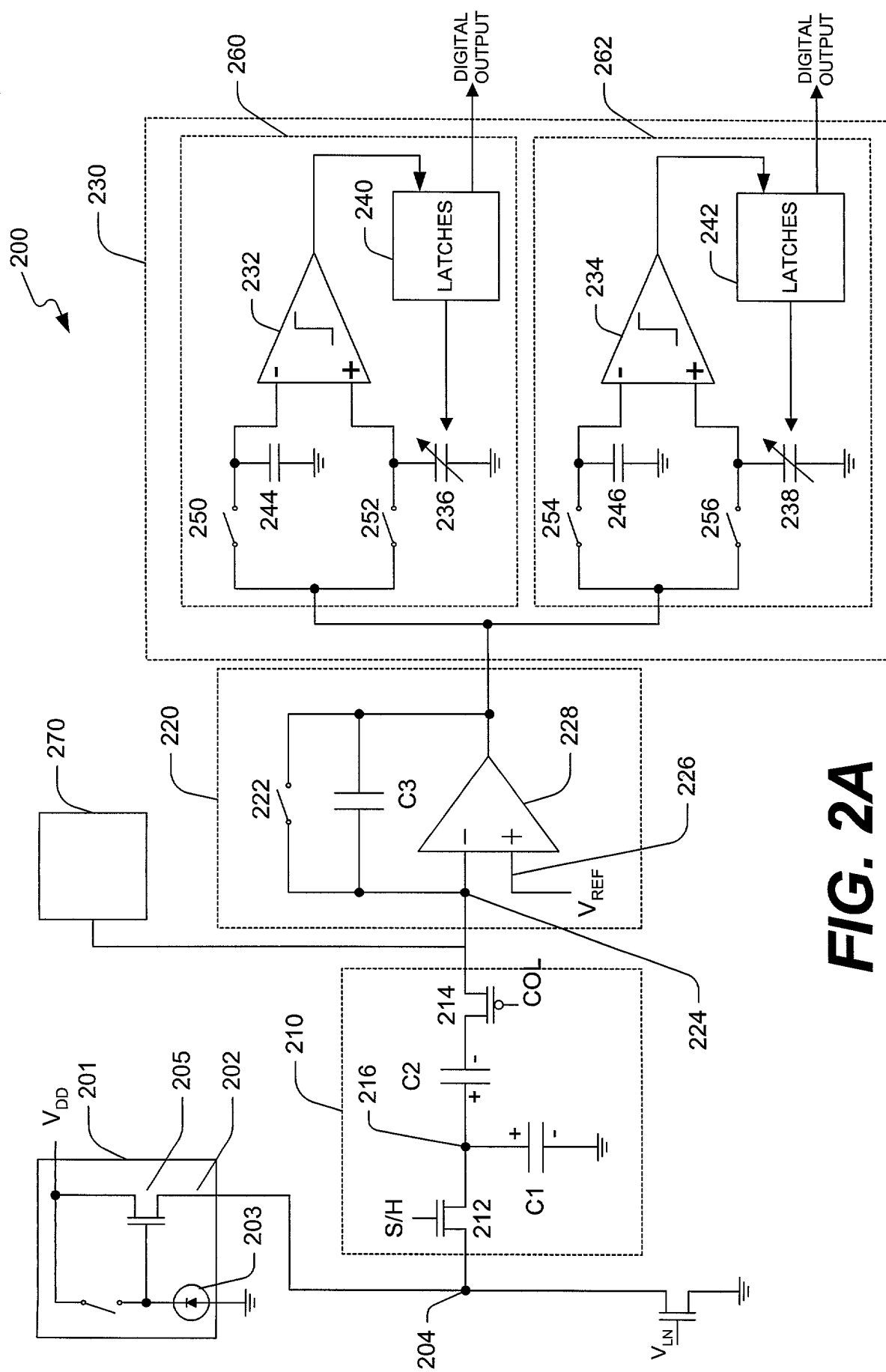


**ABSTRACT**

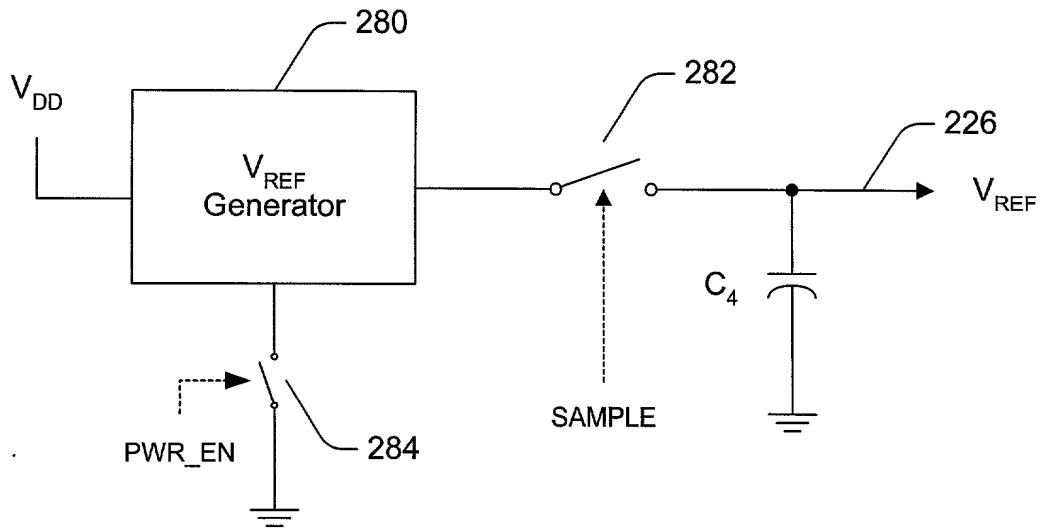
A signal chain for an image sensor is disclosed. The signal chain includes photo sensing elements, pixel readout circuits, and an amplifier. Each pixel readout circuit receives a charge-induced signal and a reset signal from one of the photo sensing elements. The readout circuit computes a difference signal between the charge-induced signal and said reset signal. The difference signal is measured with respect to a reference signal. The amplifier is coupled to the pixel readout circuits, and configured to supply the reference signal during computation of the difference signal. Further, the amplifier amplifies the difference signal when the computation is done.

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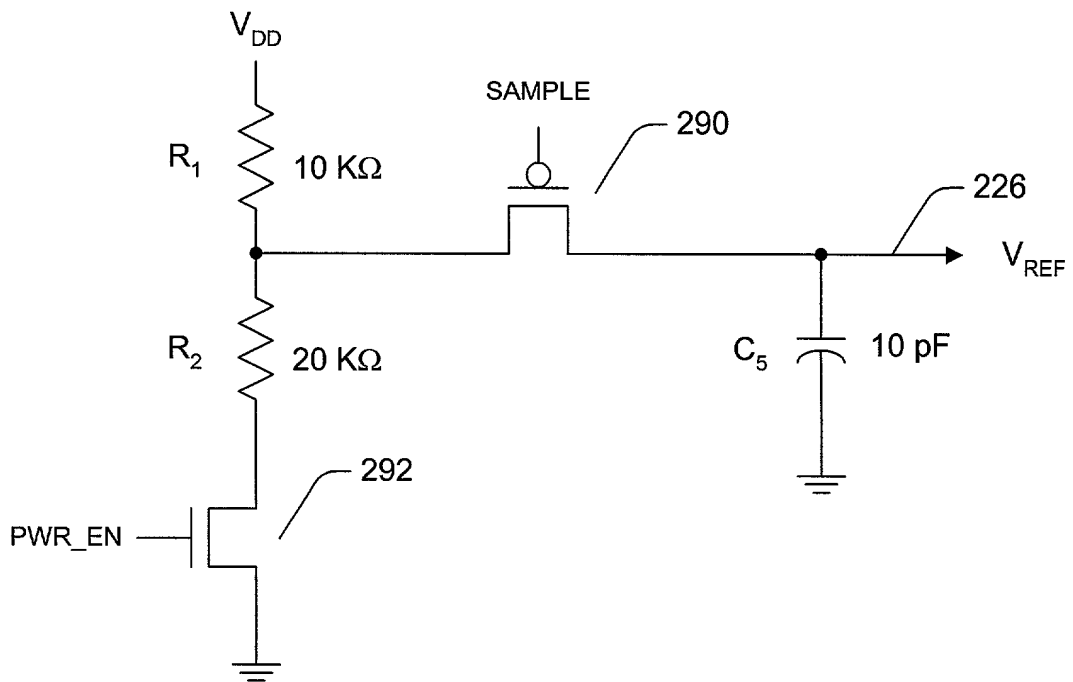




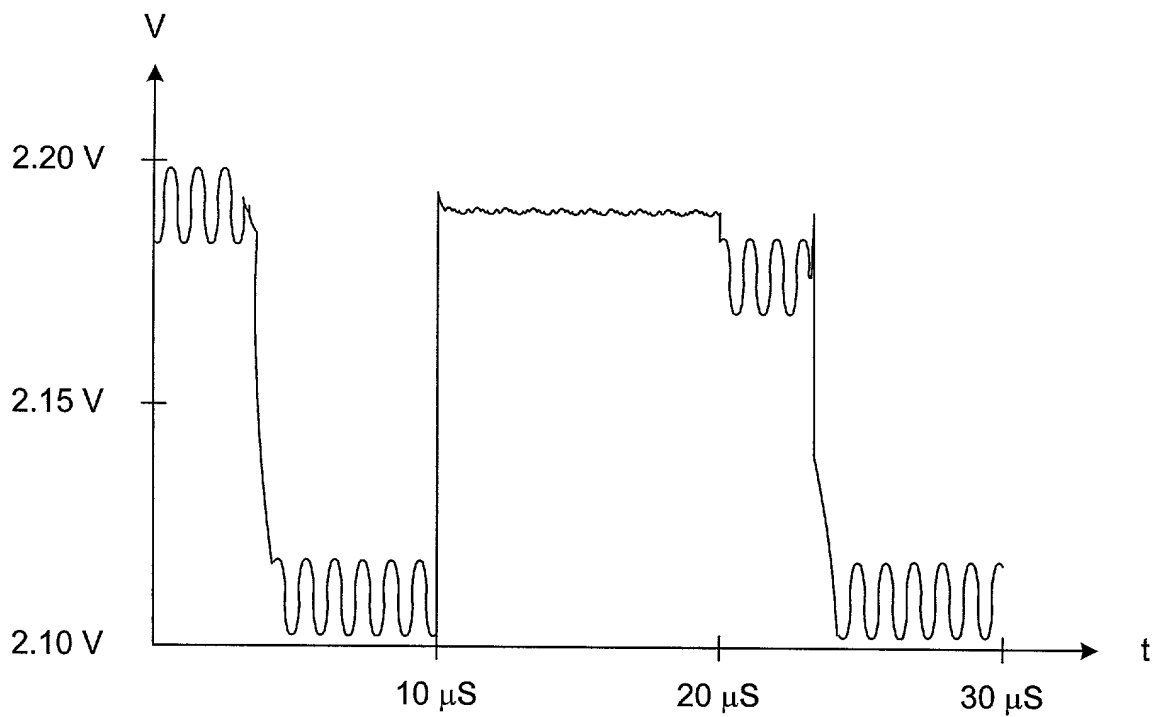
**FIG. 2A**



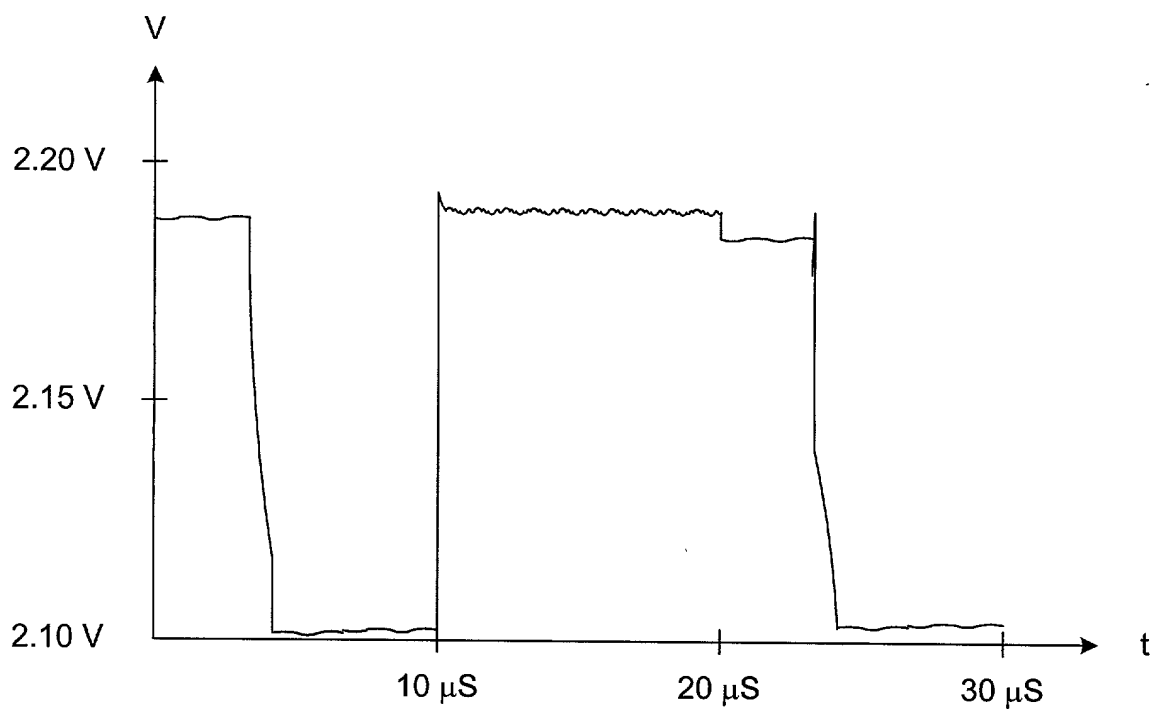
**FIG. 2B**



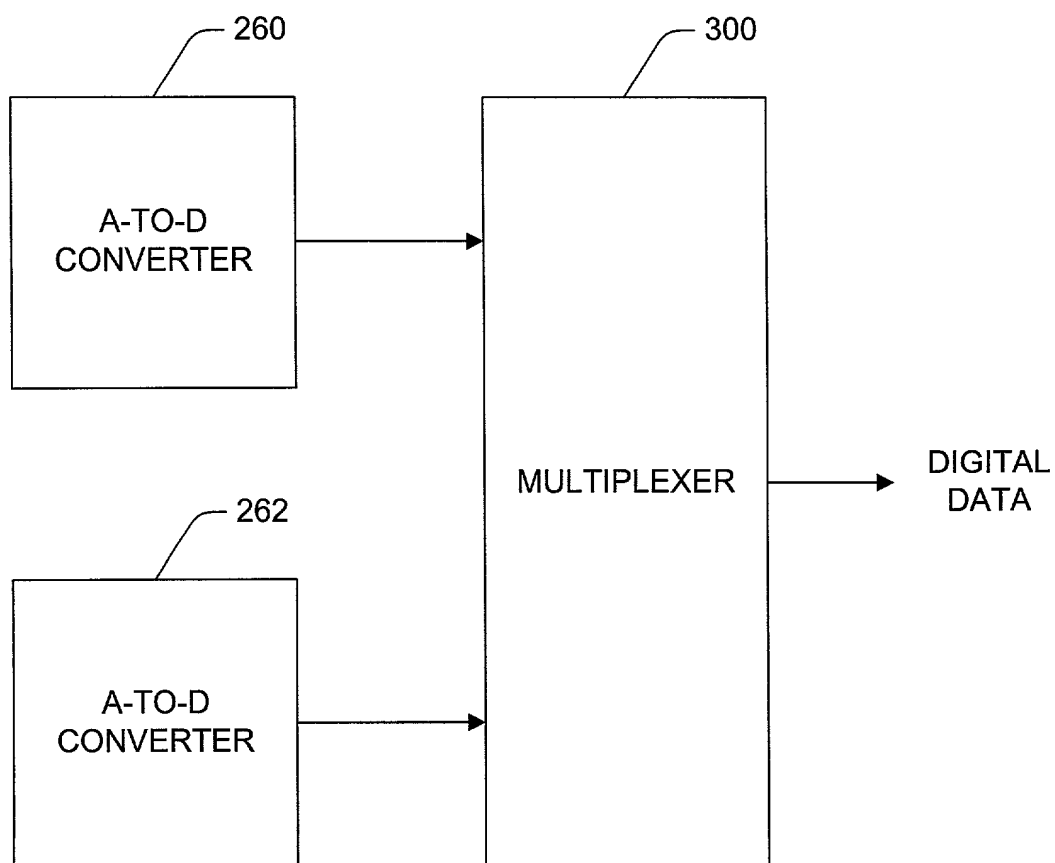
**FIG. 2C**



**FIG. 2D**



**FIG. 2E**

[illegible]

**FIG. 3**



**FIG. 5**



**COMBINED DECLARATION AND POWER OF ATTORNEY**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A LOW-POWER SIGNAL CHAIN FOR IMAGE SENSORS, the specification of which:

- ☒ is attached hereto.  
☐ was filed on \_ as Application Serial No. \_ and was amended on \_\_\_\_\_.  
☐ was described and claimed in PCT International Application No. \_\_\_\_\_ filed on \_\_\_\_\_ and as amended under PCT Article 19 on \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status
-----------------	-------------	--------

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status
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I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed
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08590785-060800

Attorney's Docket No.: 08305/081001/98-29

**Combined Declaration and Power of Attorney**

Page 2 of 2 Pages

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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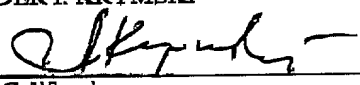
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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